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TIME DIVISION MULTIPLEX FRAME SYNCHRONIZATION: ACQUISITION, MAINTENANCE AND REACQUISITION

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A technique that can be employed to analyze the performance of proposed frame synchronization methods is presented. Candidate frame sync algorithms have two modes of operation: acquisition and verification. A time-invariant Markov chain approach is used to model the state of the synchronization process for any time period beyond an assumed initial state. An example problem, demonstrating a number of special, computational adaptations, was worked. Although the use of only a single sync

bit per frame is illustrated, the approach can be extended to a broader class of problems.

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DESCRIPTION OF TDM FRAME SYNCHRONIZATION

1.1 Introduction

Time division multiplexing (TDM) is one of the techniques used to transmit many low information rate (narrowband) channels over a single, broadband communication link. TDM usually consists of a time-ordered, channel-by-channel interleaving of digital message bits into a composite bit stream. In addition to information bits, it is essential that the multiplexer inserts "framing" bits. They enable the remote demultiplexer to synchronize with the multiplexer and direct the individual information streams to their appropriate, separate paths. The information is normally structured or strung together into regular, formatted data patterns called frames. An M-bit frame contains at least one framing bit, perhaps more. For the sake of easier treatment (which can be expanded, if necessary), this work concentrates upon those cases where only one bit per frame is required.[1] That bit appears in the same time position for each frame. Standard practice calls for the sequence of consecutive framing bits to form a repetitive pattern, the simplest being "...10 1010..." Detection of this pattern by the demultiplex unit is used in frame sync acquisition, verification (maintenance) and reacquisition. The purpose of this report is to demonstrate a useful procedure for the analysis of a class of straightforward frame synchronization algorithms.

1.2 Acquisition

Frame synchronization is initially acquired by examining (or "scanning") independent sequences of candidate frame bits until detection occurs. Any two bits in a given sequence are separated by IxM bit periods, where I is an integer and M is the number of bits per frame. Each independent sequence has a different time (or phase) relationship with respect to true frame synchronization. Acquisition is declared when one of the sequences being examined has a sufficiently high correlation with the repetitive frame bit pattern.

1.3 Verification

To detect false frame synchronization after acquisition has been declared, as well as possible loss of sync due-to bit count

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1. For a treatment of multi-bit frame synchronization codes, see, for example, References 1 and 2.

slippage, the demultiplexer continues to examine the frame bits and correlate them with the frame pattern, hereafter assumed to be the alternating one-zero pattern, identified above. If too many frame bits fail to match the alternating sequence, then the demultiplexer goes into a reacquisition mode.

1.4 Reacquisition

If, for any reason, the frame sync verification operation reveals the loss of sync, then a search, very similar to the acquisition mode, begins. However, that search should start with the examination of potential framing bit positions that are adjacent (in phase relationship) to those of the previously acquired framing pattern, including a double check of the original phase position. This foreshortens the search when only a few bit positions are lost, or when the declaration of loss of frame sync is incorrect, due to an excessive number of received bit errors, coming in a burst.

SECTION II

PROBLEM FORMULATION AND ASSUMPTIONS

2.1 Specifications

To suit different operational needs, frame synchronization can be expected to have specifications for time to acquire, time period over which correct frame synchronization is maintained, and time to reacquire frame synchronization after a loss of sync. To be complete, a specification must state the random bit error rate environment that is assumed and the required probabilities of acquisition, maintenance and/or reacquisition, within specified times. Section 4.2.2 provides example specifications.

2.2 Two Modes

Of the three types of frame sync specifications, acquisition and reacquisition are very closely related. In both cases, sequences of bits which may or may not be frame bits are examined. Therefore, during acquisition and reacquisition, it shall be assumed that the search operations are essentially the same. Sync maintenance, on the other hand, is a different problem: During verification, a set of bits which is known [or assumed] to be frame bits is examined. No others are considered. Furthermore, rather than having an objective of speed, that of certainty has more pertinence to verification goals. Consequently, it is reasonable to expect that any frame sync verification algorithm will involve a greater number of frame bit examinations than acquisition or reacquisition because there is less urgency about making a fast decision. Thus, it can be reasoned that frame synchronization entails two distinct modes of operation: acquisition and verification.

2.3 Maintenance

The problem of frame sync maintenance involves only the verification mode. The mechanism by which correct frame synchronization fails to be maintained is the occurrence of too many bit errors in the received frame sequence. This causes a switch to the acquisition mode which initially may abandon correct sync alignment. Bit slippage, due to loss of bit timing phase lock in the digital receiver, is treated as the reacquisition problem.[2] Therefore, the

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2. Thus, the initial part of the reacquisition process is the detection of the loss of frame synchronization, for which the verification mode is intended. The maintenance problem is defined as one

frame sync maintenance problem can be stated as follows: Assuming that receiver bit timing remains locked to that of the transmitter, how long will the receiver demultiplex unit remain in frame sync when there are bit errors among the received framing bits?

2.4 Acquisition and Reacquisition

The problems of frame sync acquisition and reacquisition involve both the acquisition mode and the verification mode. The verification mode is needed to protect against false synchronization due to the possible random occurrences of sync patterns within the data stream or loss of bit count integrity (BCI) by the digital data receiver. Because the verification mode is called upon to confirm true synchronization, it is part of the acquisition process and cannot totally sacrifice speed for certainty, as implied in 2.2. Thus, there is a speed/certainty tradeoff to be considered for the verification mode, just as there is one for the acquisition mode. However, the balance is tilted more towards certainty for verification than it is for acquisition.

2.5 Purely Random Data and Bit Errors

In spite of the burst nature of bit error patterns on many communication channels and the correlated (not entirely random) nature of many information bit streams, it is nevertheless assumed that all data bits are statistically independent, having 0.5 probabilities of occurrences of 0 and 1, and that all bit errors, caused during transmission, are also independent Bernoulli trials where the error probability is treated as a constant. These randomness assumptions are helpful because they can be (1) simulated during laboratory testing, (2) most easily used to analyze frame synchronization performance, and (3) considered to be a reasonably good test of the frame synchronization algorithms.

In some cases, the actual performance will be far better than the results based on these assumptions. Consider, for example, the case of a channel not being used (either temporarily or permanently). One may assume that the information stream for that channel is either all zeros or all ones (it makes little difference.). Furthermore, the format of the TDM frame will be such that bits from the unused (or any other) channel will occur periodically, either at the frame rate or some integer multiple of it, with a fixed phase relationship to the framing bit times. Therefore, if the demultiplex circuits take samples of the total bit stream at the frame rate (or multiples of it), searching for correlations with a 1010... framing pattern, it is far less likely that sync will be declared

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where a failure to verify sync is incorrect.

erroneously for the channel whose bits are constant than for a channel whose bits are random.[3] Thus, the assumption of randomness is often a very conservative one. However, it is one that is well suited for the purposes of these analyses.

2.6 Sequential Search

If the sole concerns of frame synchronization were speed and accuracy, then it is obvious that the preferred approach would be to simultaneously monitor all possible alignments (phases) of the framing pattern. For a frame whose length (including framing bit) is M, the acquisition and verification algorithms would perform their correlations with the full set of M interleaved sequences. However, maintaining M sets of records and examining all of them requires considerably more complex and expensive hardware than a sequential search.

A sequential search is one in which only a single alignment of framing is under consideration at any given time. Its major advantage is the reduced memory (by a factor of M) and processing complexity of the synchronization hardware. Moreover, if the frame sync specifications (See 2.1.) are such that a sequential search will meet the operational requirements, then it is entirely unnecessary to increase hardware expense. If an analysis of sequential techniques indicates a failure to meet user requirements, then (and only then) would one consider parallel searches: First, two framing alignments at once; then, three alignments;... until it is determined that the requirements can be met.

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3. Conversely, certain data transmissions may possess alternating patterns, forcing a different choice of framing pattern (e.g.,11001 100...).

SECTION III

ANALYSIS

3.1 Algorithms and Probabilities

As discussed in 2.2, there are two modes: acquisition and verification. In either mode, a given alignment or phasing of framing bits is initially assumed. The algorithm then examines a specified number or "window" of consecutive candidate frame bits, seeking correlation with the correct frame bit pattern. If it is determined that all but a specified number (or less) of the candidate frame bits match the synchronization sequence, then acquisition (or verification, if in the verification mode) is declared and the mode changes to (or remains in) verification; the frame bit alignment is held constant. If it is determined that too many (more than a preselected number of) bits fail to match the sequence, then the mode remains in acquisition (or reverts to it, if initially in verification); the frame bit alignment is changed (possibly by different amounts, depending upon the previous mode, acquisition or verification -- See 3.3.1.2.). The probabilities formulated below give the likelihoods of declaring acquisition or verification, either correctly or incorrectly.

3.1.1 Acquisition Mode Probabilities

Let the number of frame bits in an acquisition window be designated as N. Furthermore, let n be the maximum number of mismatches permitted to occur without preventing acquisition from being declared. If p is the probability of an error for any received bit and the probability of a 1 or a 0 in any given non-frame bit is 1/2, then the probabilities associated with the acquisition mode are calculated as follows:

3.1.1.1 Probability of Acquisition, P(ACQ)

If the frame bit timing alignment under consideration is correct, then the probability of correctly declaring acquisition is the probability that n or fewer bit errors occur among the N frame bits examined:

$$P(ACQ) = \sum_{i=0}^{n} \binom{N}{i} p^i (1-p)^{N-i} + \sum_{i=N-n}^{N} \binom{N}{i} p^i (1-p)^{N-i}, \qquad (1)$$

where

$$\binom{N}{i} = \frac{N!}{i!(N-i)!}, \qquad (2)$$

the binomial coefficient, and n is less than N/2. Note the second summation in equation (1), signifying that acquisition is declared when N-n or more bit-errors occur. This stems from the fact that frame sync acquisition could be declared for a 1010... sequence or a 0101... sequence. Especially for initial acquisition, there is no way of determining whether the 1010... sequence or its complement will be the one that is detected. For example, an eight-bit sequence, 10101010, having seven bit-errors, 01011101, appears to be an eight-bit segment of the continuous framing sequence with a single error. Fortunately, realistic values of parameters n, N, and p yield probabilities for N-n or more errors that are infinitesimally small. Consequently, the second term in equation (1) can be realistically ignored.

Note that the properties of the binomial distribution allow equation (1) to be rewritten (for computation purposes) as:

$$P(ACQ) = 1 - \sum_{i=n+1}^{N-n-1} \binom{N}{i} p^i (1-p)^{N-i}. \qquad (3)$$

3.1.1.2 Probability of a Miss, P(MISS)

Frame sync acquisition will be missed if there are more than n bits (and fewer than N-n bits) in error to corrupt the receipt of the N bits in the acquisition window:

$$P(MISS) = \sum_{i=n+1}^{N-n-1} \binom{N}{i} p^i (1-p)^{N-i}. \qquad (4)$$

Clearly, P(MISS) is the complement of P(ACQ):

$$P(ACQ) + P(MISS) = 1. \qquad (5)$$

3.1.1.3 Probability of False Acquisition, P(FA)

The probability that the acquisition algorithm will detect the framing sequence among [assumed] random, non-frame bits is determined in the same manner as equation (1), except that the probability of bit mismatch is 1/2, instead of p, and the probability of bit match is also 1/2, instead of 1-p. Thus, one gets

$$P(FA) = \sum_{i=0}^{n} \binom{N}{i}(.5)^i(.5)^{N-i} + \sum_{i=N-n}^{N} \binom{N}{i}(.5)^i(.5)^{N-i}, \quad (6)$$

$$= 2^{-N}\left[\sum_{i=0}^{n}\binom{N}{i} + \sum_{i=N-n}^{N}\binom{N}{i}\right], \quad (7)$$

$$= 2^{-N}\left[\, 2\cdot\sum_{i=0}^{n}\binom{N}{i}\right], \quad (8)$$

$$= 2^{-(N-1)}\sum_{i=0}^{n}\binom{N}{i}, \quad (9)$$

where the transition from expression (7) to (8) is attributable to the symmetry of the binomial coefficients (See equation (2).).

3.1.1.4 Probability of Correctly Ignoring Data, P(I)

Following the discussions in 3.1.1.2 and 3.1.1.3, it should be obvious that P(I) is defined by:

$$P(I) = 1 - P(FA) \quad (10)$$

and also given by

$$P(I) = 1 - 2^{-(N-1)}\sum_{i=0}^{n}\binom{N}{i} \text{ or} \quad (11)$$

$$P(I) = 2^{-N}\sum_{i=n+1}^{N-n-1}\binom{N}{i}. \quad (12)$$

3.1.2 Verification Mode Probabilities

The only differences between the expressions obtained for the acquisition mode and those for verification are the length of the verification window, L, and the number of mismatches that are tolerated, l. Consequently, the results are entirely analogous to those presented in 3.1.1, above:

3.1.2.1 Probability of Correct Verification, P(V)

$$P(V) = \sum_{i=0}^{\ell} \binom{L}{i} p^i (1-p)^{L-i} + \sum_{i=L-\ell}^{L} \binom{L}{i} p^i (1-p)^{L-i}, \tag{13}$$

$$= 1 - \sum_{i=\ell+1}^{L-\ell-1} \binom{L}{i} p^i (1-p)^{L-i}. \tag{14}$$

3.1.2.2 Probability of Loss of Synchronization, P(LOSS)

$$P(LOSS) = \sum_{i=\ell+1}^{L-\ell-1} \binom{L}{i} p^i (1-p)^{L-i}, \tag{15}$$

$$= 1 - P(V). \tag{16}$$

3.1.2.3 Probability of Incorrect Verification, P(NV)

$$P(NV) = \sum_{i=0}^{\ell} \binom{L}{i} (.5)^i (.5)^{L-i} + \sum_{i=L-\ell}^{L} \binom{L}{i} (.5)^i (.5)^{L-i}, \tag{17}$$

$$= 2^{-L} \left[\sum_{i=0}^{\ell} \binom{L}{i} + \sum_{i=L-\ell}^{L} \binom{L}{i} \right], \tag{18}$$

$$= 2^{-L} \left[2 \cdot \sum_{i=0}^{\ell} \binom{L}{i} \right], \tag{19}$$

$$= 2^{-(L-i)} \sum_{i=0}^{\ell} \binom{L}{i}. \tag{20}$$

3.1.2.4 Probability of Detection of False Sync, P(VFS)

$$P(VFS) = 1 - P(NV), \tag{21}$$

$$= 1 - 2^{-(L-1)} \sum_{i=0}^{\ell} \binom{L}{i}, \tag{22}$$

$$= 2^{-L} \sum_{i=\ell+1}^{L-\ell-1} \binom{L}{i}. \tag{23}$$

3.2 Maintenance

As discussed in 2.3, frame sync maintenance involves only the verification mode. Maintenance probabilities give the likelihoods that correct frame synchronization will be maintained in spite of received bit errors. The probability that frame synchronization will be maintained for at least Q verification windows (QxL frames) is the probability that correct verification occurs Q windows in a row:

$$P(M_Q) = [P(V)]^Q, \tag{24}$$

$$= [1-P(LOSS)]^Q, \tag{25}$$

where P(V) and P(LOSS) are defined in 3.1.2.1 and 3.1.2.2, respectively.

3.3 Acquisition and Reacquisition

3.3.1 Markov Chain Approach

3.3.1.1 System States

At any given time during the search for frame sync [re]acquisition, the processing logic examines a sequence of received bits that are candidate framing bits, spaced at M-bit intervals. Relative to correct frame synchronization, the alignment of the candidate framing sequence can take on any one of M possible positions, including true alignment. When in the acquisition mode, each of the M possible alignments can be considered a separate system state.

For M-1 of those acquisition mode states, there is a finite probability (P(FA) -- See 3.1.1.3.) that frame sync acquisition will be declared incorrectly. Unaware of the false sync condition, the processing logic enters the verification mode. At that point, the false sync condition will either be detected (with probability P(VFS) -- See 3.1.2.4.) or incorrectly [re]verified (with probability P(NV) -- See 3.1.2.3.). The M-1 false alarm/verification mode

states that are associated with the M-1 non-aligned acquisition mode states constitute an additional set of M-1 states.

For the single acquisition mode state that corresponds to correct frame alignment, sync acquisition will either be declared correctly (with probability P(ACQ) -- See 3.1.1.1.) or missed (with probability P(MISS) -- See 3.1.1.2.). Correct declaration of acquisition puts the system into a terminal, absorption state, namely ACQuisition. Thus, there are 2xM possible states in which the search logic can find itself: M acquisition mode search states, M-1 false acquisition/verification mode states, and the ACQuisition state.

3.3.1.2 State Transitions

Figure 1 presents a partial representation of the state transition diagram for the 2xM-state Markov chain that is being modeled. The remaining model formulations to be made involve the identification of acquisition states to which the system transitions when false sync is discovered in any of the M-1 false alarm/verification mode states, F_i. Otherwise, the transition diagram summarizes the following information:

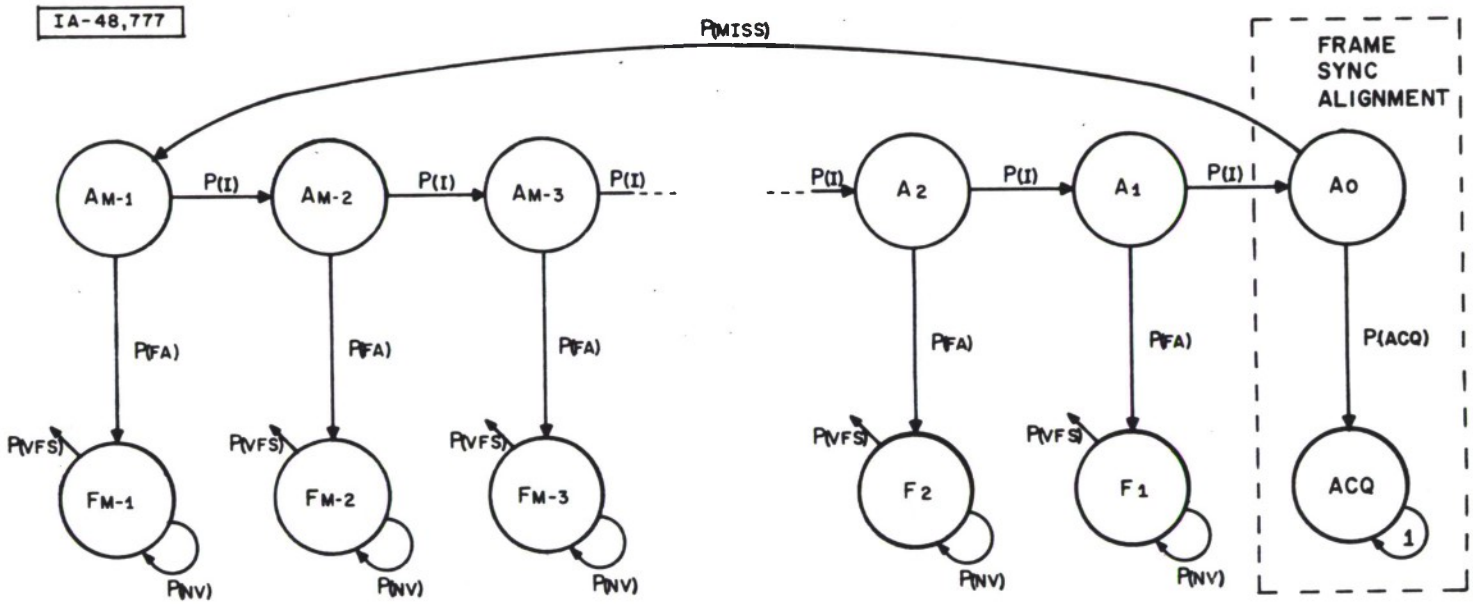
(1) When frame non-alignment is correctly discovered in one of M-1 "out-of-sync" acquisition mode states (A_1, A_2, ...A_{M-1}), the state transition is to the next [lowest] acquisition mode state (A_0, A_1,....A_{M-2}), closer to, if not directly in, frame sync alignment. It is natural to assign state numbers (e.g., i, as in A_i) to correspond to the number of bit positions that the state is away from true alignment.[4]

(2) When frame alignment is incorrectly missed while in the aligned acquisition state, A_0, the transition is to state A_{M-1}. This follows from the periodicity of the framing format.

(3) When false acquisition is incorrectly [re]verified while in one of the false alarm/verification mode states, the processing logic remains in that state.

(4) When in the ACQ state, Figure 1 indicates that there is no sync loss (i.e., frame synchronization is permanently maintained). To be completely accurate, the probability for the

4. It need not be specified whether the number of bits away from correct alignment means bit positions preceding (in time) or following the frame bit position. The differences in resulting [re]acquisition times are not significant (on the order of one frame period, on average).



LEGEND:

Ai — ACQUISITION MODE STATE, i BIT POSITIONS AWAY FROM FRAME SYNC ALIGNMENT

Fi — FALSE ALARM/VERIFICATION MODE STATE, i BIT POSITIONS AWAY FROM FRAME SYNC ALIGNMENT

ACQ— ACQUISITION (ABSORPTION) STATE

Figure 1. STATES AND TRANSITION PROBABILITIES FOR THE FRAME SYNC ACQUISITION/REACQUISITION MODEL

transition from ACQ back to itself is P(V) (See 3.1.2.1.); the transition out of ACQ has a probability of P(LOSS) (See 3.1.2.2.) and follows the same rule (not yet indicated) that applies to transitions out of the false alarm/verification mode states. However, real values of P(LOSS) will be extremely low and the purpose of the Markov model is to determine the probability and time to the first [re]acquisition. Therefore, the transition probability of 1 (complete absorption) is employed.

The particular acquisition mode state to which the system transitions when leaving a given verification mode state depends upon reacquisition considerations. If a demultiplexer achieves correct frame synchronization and then loses it because of loss of bit count integrity (BCI), it is likely that the amount of bit slippage is no more than a single bit position, or two. In the state transition diagram (Figure 1), this corresponds to an abrupt state change from ACQ to state F_1, F_{M-1} (slippage of one bit), F_2, or F_{M-2} (slippage of two bits). If the maximum amount of bit slippage is assumed to be two bit positions, then it would be desirable to make the rule that verification of false synchronization would cause the sync search to go back two bits (e.g., F_2 to A_4, F_1 to A_3, F_{M-1} to A_1, and F_{M-2} to A_0). Thus, the likelihood of having to pass through states A_{M-1}, A_{M-2}, A_{M-3}, etc. would be greatly reduced, as would the mean time to reacquire synchronization. Therefore, the optimum state transition algorithm depends, to some extent, on the receiver's bit synchronization capabilities. [To be consistent with the example in Section IV, a maximum slippage of two bit positions will hereafter be assumed.]

3.3.2 Markov Chain Modification

To facilitate easy, straightforward computation of the Markov chain analysis, it is desirable to work with states whose time durations are equal. This enables one to determine the precise state of the system[5] at any time after a known, initial system state. In those cases where the acquisition mode window length, N, differs from the length of the verification mode window, L, the time spent in any of the M acquisition mode states, A_i, i=0,1...M-1, will not be the same as the time duration of any one of the M-1 false alarm/verification mode states, F_i, i=1,2,...M-1. Therefore, the approach of dividing the A and F states into substates whose lengths are equal to the largest common integer factor of N and L will yield Markov chain states that lend themselves to the traditional

5. "State of the system" is hereafter defined as the set of probabilities (whose total is 1) of the acquisition logic finding itself in any of the Markov chain states, each of which has a probability associated with it.

transition probability matrix approach (See, for example, References 3-5.). The Appendix describes the computational approach in greater detail.

SECTION IV

EXAMPLE PROBLEM

4.1 Objective

The example problem that is analyzed using the Markov chain approach, developed in Section III, has TDM parameters and specifications that are comparable with those of the multiplex section of one version of a digital microwave radio that is currently being considered for a Defense Communication System (DCS) application. Consequently, the results, although not necessarily applicable to the actual DCS problem (due to several simplifications), give an indication of the achievable performance, relative to specifications. In addition to the insights into synchronization performance that can be gained, the major purpose of this example is to demonstrate the manner in which the problem is attacked and the computational methods that are called on.

4.2 Problem Details

4.2.1 TDM Parameters:

(a) Number of bits per frame, M = 70
(b) Number of frames per second = 192,000
(c) Number of bits per second = 70 x 192,000 = 1.344×10^7

4.2.2 Specifications

4.2.2.1 Time to Acquire Frame Sync. At a bit error rate (BER) of 10^{-3}, frame sync shall be acquired within 10 milliseconds, with a probability of 0.90.

4.2.2.2 Time to Reacquire Frame Sync. At a BER of 10^{-3}, loss of frame sync shall be detected and correct sync reacquired within 10 milliseconds, with a probability of 0.90, provided that the received data and TDM are within two bits of synchronism.

4.2.2.3 Probability of Frame Sync Maintenance. At a BER of 10^{-2}, frame sync shall not be declared lost due to bit error count for a period greater than 24 hours, with a probability of 0.90.

4.3 Approach

Having established the concepts of acquisition and verification windows, allowed bit errors per window, and sequential search, much

of the approach to the design of the synchronization algorithm is complete. The remaining optimization problems are the selection of parameters: N, n, L and l, plus the identification of the new frame sync bit alignment after false synchronization is detected (as discussed in 3.3.1.2).

4.3.1 Transition from Verification Mode to Acquisition Mode

The discussion of state transitions (3.3.1.2), in conjunction with the reacquisition specification (4.2.2.2), indicates that the logical transition from one of the false verification states (F_1 through F_{M-1}, as depicted in Figure 1) to one of the acquisition states (A_0 through A_{M-1}) would be to go back two bits in the frame sync search: F_i to A_{i+2}, $1 \leq i \leq M-3$; F_{M-2} to A_0; and F_{M-1} to A_1. Thus, any one- or two-bit displacement from state ACQ to state F_2, F_1, F_{M-1} or F_{M-2} would, upon detection of false synchronization, lead to state A_4, A_3, A_1 or A_0, respectively. The expected time to reacquire synchronization (transition to state ACQ) should then be minimized.

4.3.2 Pairing Verification Parameters L and l

Prior to embarking on a four-dimensional search over N, n, L and l, it is worthwhile to consider that the acquisition mode parameters, N and n, pertain only to the acquisition/reacquisition problem, whose performance goal is measured in terms of speed, while the verification mode parameters, L and l, affect the performance of acquisition/reacquisition, as well as maintenance, whose performance objective is measured in terms of certainty (See 2.2.). Consequently, the choice of parameters L and l will have to result from a compromise of somewhat contrary objectives. The approach taken for this example is to determine, for each verification window length, L, the minimum number of permitted mismatches, l, that still allows satisfaction of the maintenance specification (4.2.2.3). It is desirable to minimize l in order to increase the probability of detecting false sync (in a given window, L), P(VFS), and speeding the acquisition/reacquisition process. Figure 2 graphically presents computed 24-hour frame sync maintenance probabilities for the example problem in terms of L and l. From those results, the value of l to be employed with any given choice of L can be determined. Table I presents the resulting pairs of L and l.

4.3.3 Minimizing Acquisition and Reacquisition Times

For any value of L, Table I indicates the minimum (best, from a frame sync acquisition point of view) value of l that still permits satisfaction of the frame sync maintenance specification, 4.2.2.3. Selection of L automatically specifies l. Consequently, the

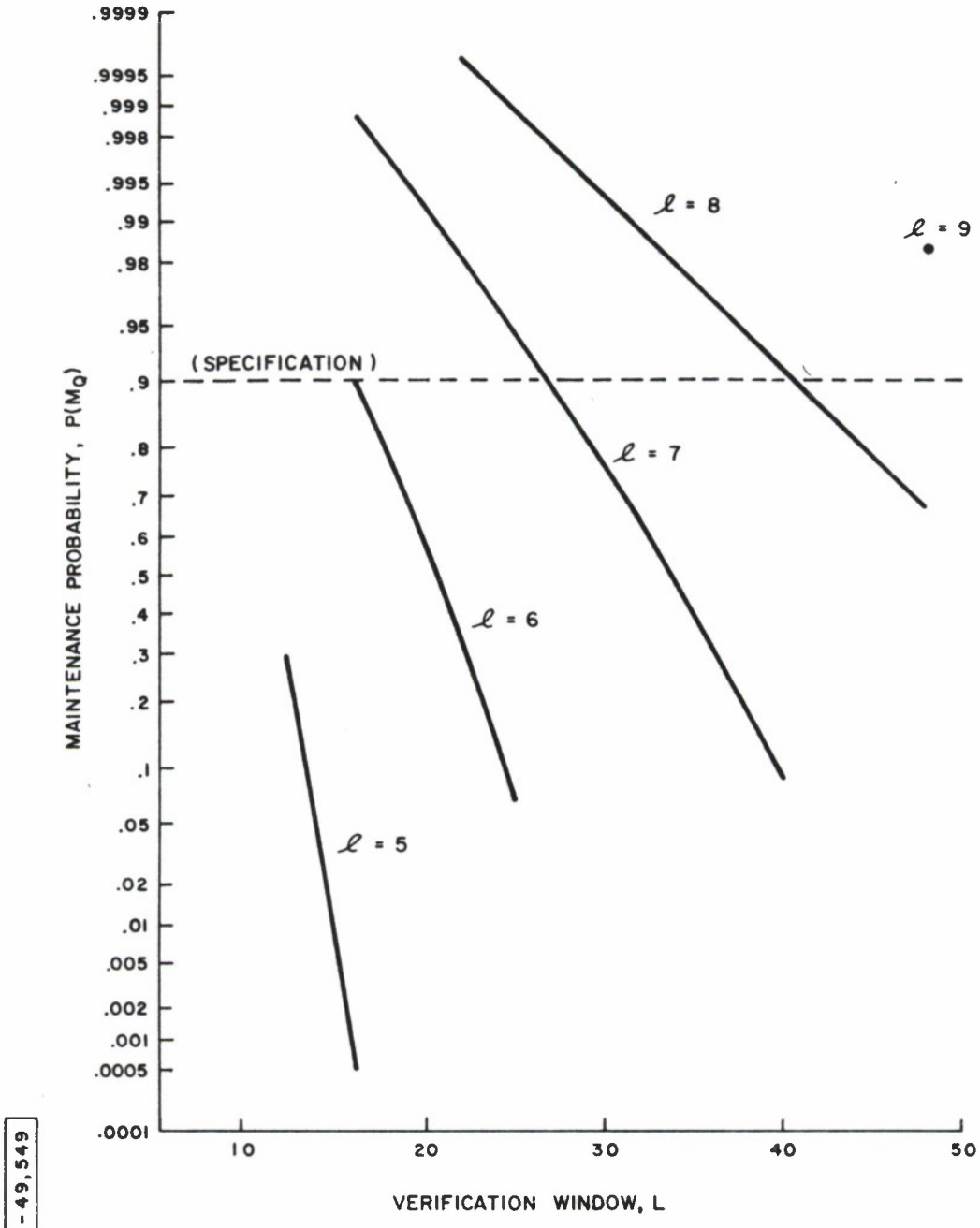


Figure 2 . 24-HOUR FRAME SYNC MAINTENANCE PROBABILITIES
(BER = 10^{-2})

Table I - Pairs of L and l

Values of L (Verification Window Size)	Minimum [Preferred] l (Allowed Number of Mismatches)
13 - 15	6
16 - 26	7
27 - 41	8
42 - 48+	9

minimization of acquisition and reacquisition times becomes a three-parameter search, over N, n and L. The key techniques used to calculate the [re]acquisition probabilities resulting from the search parameters are presented in the Appendix.

4.4 Results

Initial trials (N=32, n=6 and L=48) indicated that the proposed specification for acquisition (4.2.2.1) and reacquisition (4.2.2.2) could be met by a sequential search (See 2.6.). Therefore, the computer program was amended to include the calculation of expected (mean) time to [re]acquire sync. Rather than optimizing the probability of [re]acquiring within 10 milliseconds (which very closely approaches 1), the minimization of expected time to [re]acquire sync was found to be capable of very finely differentiating among the various solutions, all of which meet the [seemingly loose] specifications. The resulting values of expected time to acquire and reacquire frame sync in the presence of a 10^{-3} BER are presented in Table II.

4.4.1 Optimum Values

Observation of the trends in Table II has led to the conclusion that the optimum selections of N, n, L, and l are 6, 0, 23 and 7, respectively. The performance resulting from those parameters is an expected acquisition time of 1389 microseconds and an expected reacquisition time (from a two-bit slip - state F_2) of 335 microseconds. Figure 3 is a graphical presentation of those data points with shorter [re]acquisition times. Note how the points having the same acquisition window size, N, tend to occur along straight lines, of constant incremental acquisition time vs. incremental reacquisition time. Also, the slopes of those lines tend to vary inversely with N. Furthermore, for the four "best" values of N (those plotted), L=23 yields the optimum performance in each case (for this particular example).

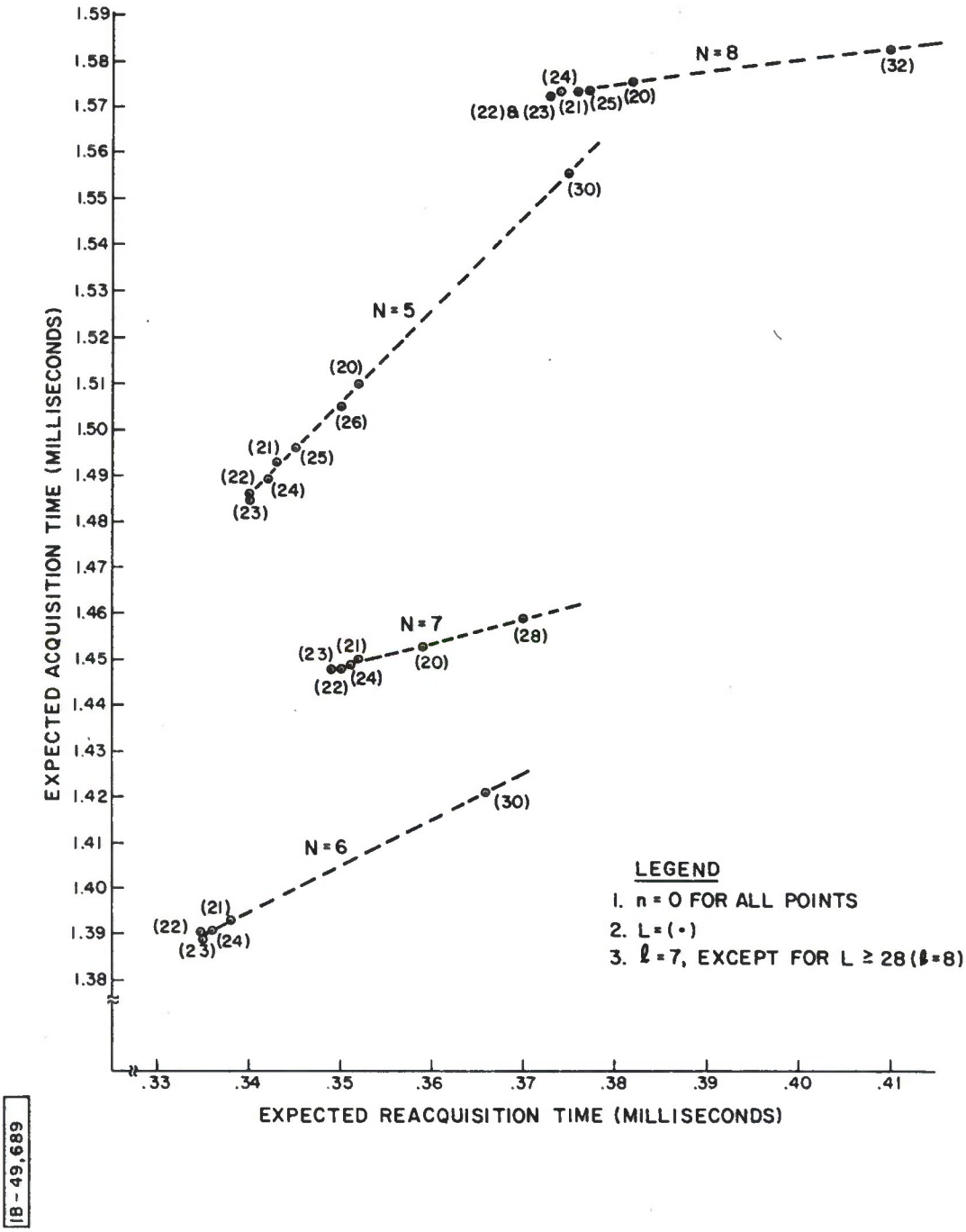


Figure 3. SHORTER (RE)ACQUISITION TIMES

Table II - Expected Acquisition and Reacquisition Times

N	n	L	l	Acq. (ms.)	Reacq. (ms.)	N	n	L	l	Acq. (ms.)	Reacq. (ms.)
16	3	16	7	3.480	0.902	*7	0	24	7	1.449	0.351
16	2	16	7	3.056	0.852	*7	0	23	7	1.448	0.349
16	2	20	7	3.014	0.565	*7	0	22	7	1.448	0.350
16	1	16	7	2.971	0.843	*7	0	21	7	1.450	0.352
16	1	20	7	2.966	0.560	*7	0	20	7	1.453	0.359
16	0	16	7	3.053	0.935	6	1	24	7	5.764	0.868
12	1	24	7	2.289	0.455	*6	0	30	8	1.421	0.366
12	0	24	7	2.277	0.500	*6	0	24	7	1.391	0.336
8	1	32	8	2.361	0.481	*6	0	23	7	1.389	0.335
8	1	24	7	2.257	0.434	*6	0	22	7	1.390	0.335
8	1	20	7	2.281	0.445	*6	0	21	7	1.393	0.338
8	1	16	7	3.144	0.829	*5	0	30	8	1.556	0.375
*8	0	32	8	1.583	0.410	*5	0	26	7	1.505	0.350
*8	0	25	7	1.574	0.377	*5	0	25	7	1.496	0.345
*8	0	24	7	1.574	0.374	*5	0	24	7	1.489	0.342
*8	0	23	7	1.573	0.373	*5	0	23	7	1.485	0.340
*8	0	22	7	1.573	0.373	*5	0	22	7	1.486	0.340
*8	0	21	7	1.574	0.376	*5	0	21	7	1.493	0.343
*8	0	20	7	1.576	0.382	*5	0	20	7	1.510	0.352
8	0	16	7	1.655	0.676	4	0	24	7	2.068	0.406
*7	0	28	8	1.459	0.370	3	0	24	7	6.204	0.947

*Plotted in Figure 3.

4.4.2 Bit Error Rate Sensitivity

Having determined the optimum parameter values and performance in a 10^{-3} bit error rate environment, it is instructive to note how well the selected frame sync algorithm will perform at other bit error rates. Table III presents those values. Increasing the BER (from 10^{-3}) does not begin to significantly increase the expected acquisition and reacquisition times until errors are far too dense for useful information transfer.

Table III - BER Sensitivity

BER	Acquisition(ms.)	Reacquisition(ms.)
10^{-4}	1.376	0.321
10^{-3}	1.389	0.335
10^{-2}	1.532	0.478
10^{-1}	3.621	2.567

4.5 Suggested Modification

In addition to the parallel search procedures discounted earlier (2.6.), one simple modification would permit the search algorithm to abandon its acquisition or verification mode state as soon as the allowable number of mismatches has been exceeded. For example, in the case of N=6 and n=0, rather than waiting for six frame intervals, a mismatch can be detected as early as the second bit sample (if it matches the first sample and the alternating sequence is being employed). In fact, the mean time spent in state A_1, A_2,... or A_{M-1} would be slightly less than three frame periods, halving the amount of search time spent in the non-aligned acquisition mode states. Although the Markov chain model would become far more complex for this modification, it remains the most useful tool for studying the candidate algorithm.

SECTION V

CONCLUSION

The Markov chain approach, used previously for analyses of other frame synchronization algorithms (References 4 and 5), has again been shown to be of practical value. One innovation used here is the assignment of states according to distance from correct frame alignment, rather than state of a complex synchronization algorithm. This permits the Markov model to have time-invariant transition probabilities. The approach can also be applied flexibly to various sync algorithms, without significant change to the basic computer model. Other useful features noted herein include the employment of substates to account for varying time delays and logarithms of probability values to maintain numerical accuracy over widely varying magnitudes. Thus, a new straightforward Markov approach has been shown to be useful in the study of frame synchronization of time division multiplexed systems.

APPENDIX

COMPUTATIONAL APPROACH

A.1 States and Substates

Because the value chosen for L is expected to be larger than N, L is expressed in terms of N:

$$L = \frac{X}{Y} \cdot N, \qquad \text{(A-1)}$$

where X and Y are the lowest possible integer values that can be used to relate L to N. This translates to each of the acquisition mode states, A_i, having Y substates (of time duration N/Y frames) and each of the verification mode states, F_i, having X substates (of time duration L/X frames). For example, suppose L=24 and N=6, then X=4 and Y=1 would be used, corresponding to substates having durations of six frames. For L=23 and N=6, X=23 and Y=6 are the lowest possible values, resulting in substates whose durations are a single frame and computation time that is greater. Consequently, the set of states that is represented in the modified Markov chain is

(a) Acquisition Mode - A(I,J): I=0,1,...M-1; J=1,2,...Y;

(b) Verification Mode - F(I,K): I=1,2,...M-1; K=1,2,...X; and

(c) Correct Acquisition - ACQ.

A.2 Transition Rules

The number associated with any substate is the probability of being in that substate for the time interval under consideration. Because all states, with the exceptions of A_2 (See 3.3.1.2.) and ACQ, can be entered from either an acquisition (A) or verification (F) state, the transition to a given state (as opposed to substate) will involve two multiplications and an addition. For example,

$$A_i \leftarrow P(VFS) \cdot F_{i-2} + P(I) \cdot A_{i+1}, \; i=3,4,...M-2, \text{ and} \qquad \text{(A-2)}$$

$$F_j \leftarrow P(NV) \cdot F_j + P(FA) \cdot A_j, \; j=1,2,...M-1. \qquad \text{(A-3)}$$

Generalizing to the substate formulations given in A.1, the transition rules become

$$A(0,Y) \leftarrow P(VFS)\bullet F(M-2,1) + P(I)\bullet A(1,1); \quad \text{(A-4)}$$

$$A(1,Y) \leftarrow P(VFS)\bullet F(M-1,1) + P(I)\bullet A(2,1); \quad \text{(A-5)}$$

$$A(2,Y) \leftarrow P(I)\bullet A(3,1); \quad \text{(A-6)}$$

$$A(I,Y) \leftarrow P(VFS)\bullet F(I-2,1) + P(I)\bullet A(I+1,1);\ I=3,4,\ldots M-2; \quad \text{(A-7)}$$

$$A(M-1,Y) \leftarrow P(VFS)\bullet F(M-3,1) + P(MISS)\bullet A(0,1); \quad \text{(A-8)}$$

$$A(I,J) \leftarrow A(I,J+1);\ I=0,1,\ldots M-1;\ J=1,2,\ldots Y-1 \text{ (only for } Y\neq 1); \quad \text{(A-9)}$$

$$F(I,X) \leftarrow P(NV)\bullet F(I,1) + P(FA)\bullet A(I,1);\ I=1,2,\ldots M-1; \quad \text{(A-10)}$$

$$F(I,J) \leftarrow F(I,J+1);\ I=1,2,\ldots M-1;\ J=1,2,\ldots X-1 \text{ (only for } X\neq 1); \quad \text{(A-11)}$$

$$ACQ \leftarrow ACQ + P(ACQ)\bullet A(0,1). \quad \text{(A-12)}$$

A.3 Logarithms

Because the probabilities that are to be stored as state variables can take on a wide range of values (from very small to very close to unity), the normal range and precision of floating point arithmetic may be inadequate. For example, a factor of the form: (1-x), where x is very small, is to be used repeatedly as a multiplier (e.g., P(I) and P(VS)). The least significant bit in a floating point number representing (1-x) equals $2^{-24} = 5.96 \times 10^{-8}$, which may be larger than some values of x that can be encountered. Therefore, as certain probabilities get very close to 1, it becomes necessary to employ an alternate approach: logarithms. The Taylor series expansion of ln(1-x) is given by

$$\ln(1-x) = \sum_{i=1}^{\infty} -\frac{x^i}{i}, \quad \text{(A-13)}$$

where ln(•) is the natural logarithm (base e). For very small values of x, it is close to -x. Consequently, for values of x that are very small, the accuracy of (1-x) is not diminished by numerical computation limitations.

Although logarithms are beneficial in cases of repeated multiplications, expressions of the form

$$f = a\bullet b + c\bullet d \quad \text{(A-14)}$$

appear as

$$\ln(f)=\ln\{\exp[\ln(a)+\ln(b)]+\exp[\ln(c)+\ln(d)]\} \qquad \text{(A-15)}$$

and use quite a bit of computer time. However, in our case, because one of the two expressions, a•b or c•d, is usually much larger than the other, equation (A-14) would reduce to either

$$f = a \bullet b \quad \text{or} \qquad \text{(A-16)}$$

$$f = c \bullet d \qquad \text{(A-17)}$$

and equation (A-15) would reduce to either

$$\ln(f)=\ln(a)+\ln(b) \quad \text{or} \qquad \text{(A-18)}$$

$$\ln(f)=\ln(c)+\ln(d). \qquad \text{(A-19)}$$

Therefore, evaluation of the expressions in (A-4) through (A-11) is not normally expected to result in (A-15).

A.4 Initial Values

A.4.1 Acquisition

For initial acquisition, the system begins to search for sync from one of the M acquisition mode states. Because of random selection, the probability of being in any one of the states is 1/M. Therefore, using natural logarithms, the initial values for the first acquisition mode substates are

$$A(I,Y) = \ln(1/M) = -\ln(M), \qquad \text{(A-20)}$$

where I=0,1,...M-1. All other acquisition mode substates, A(I,J), where $1 \leq J \leq Y-1$, are set to -1000, a sufficiently large negative number corresponding to zero probability ($\ln(0) \longrightarrow -\infty$). Similarly, all verification mode substates, F(•,•), are set to -1000.

A.4.2 Reacquisition

As discussed in 3.3.1.2, the reacquisition problem can be modeled as an abrupt slip from state ACQ to F_{M-2}, F_{M-1}, F_1 or F_2. Of these, the worst case is the shift to F_2: The transition algorithm (See 4.3.1.) reinitiates search for acquisition (after verification of false sync) in state A_4, four bits away from correct alignment (as opposed to three, one or zero). Consequently, the initial

substate values in the reacquisition problem are all -1000, except for F(2,X), which is ln(1)=0.

GLOSSARY

Bit Count Integrity (BCI) - The condition that exists wherein the precise sequence of bits that was transmitted is received, without additions or deletions.

L - number of frame bits per verification window

l - maximum acceptable number of mismatches permitted for a given verification window

M - number of bits per frame

N - number of frame bits per acquisition window

n - maximum acceptable number of mismatches permitted for a given acquisition window

p - probability of a received bit error

P(ACQ) - probability of correctly declaring frame sync acquisition for a given acquisition window

P(FA) - probability of incorrectly declaring frame sync acquisition on information (non-framing) bits

P(I) - probability of correctly determining, in a given acquisition window, that frame synchronization does not exist

P(LOSS) - probability that frame synchronization is incorrectly determined to be lost in a given verification window

P(MISS) - probability of incorrectly failing to declare frame sync acquisition for a given acquisition window

$P(M_Q)$ - probability that frame synchronization is maintained for at least Q verification windows

P(NV) - probability that, during a verification window, frame synchronization is incorrectly verified as being aligned

P(V) - probability of correctly determining, in a given verification window, that frame synchronization continues to be aligned

P(VFS) - probability that, during a verification window, false frame synchronization is correctly identified

TDM - time division multiplex

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